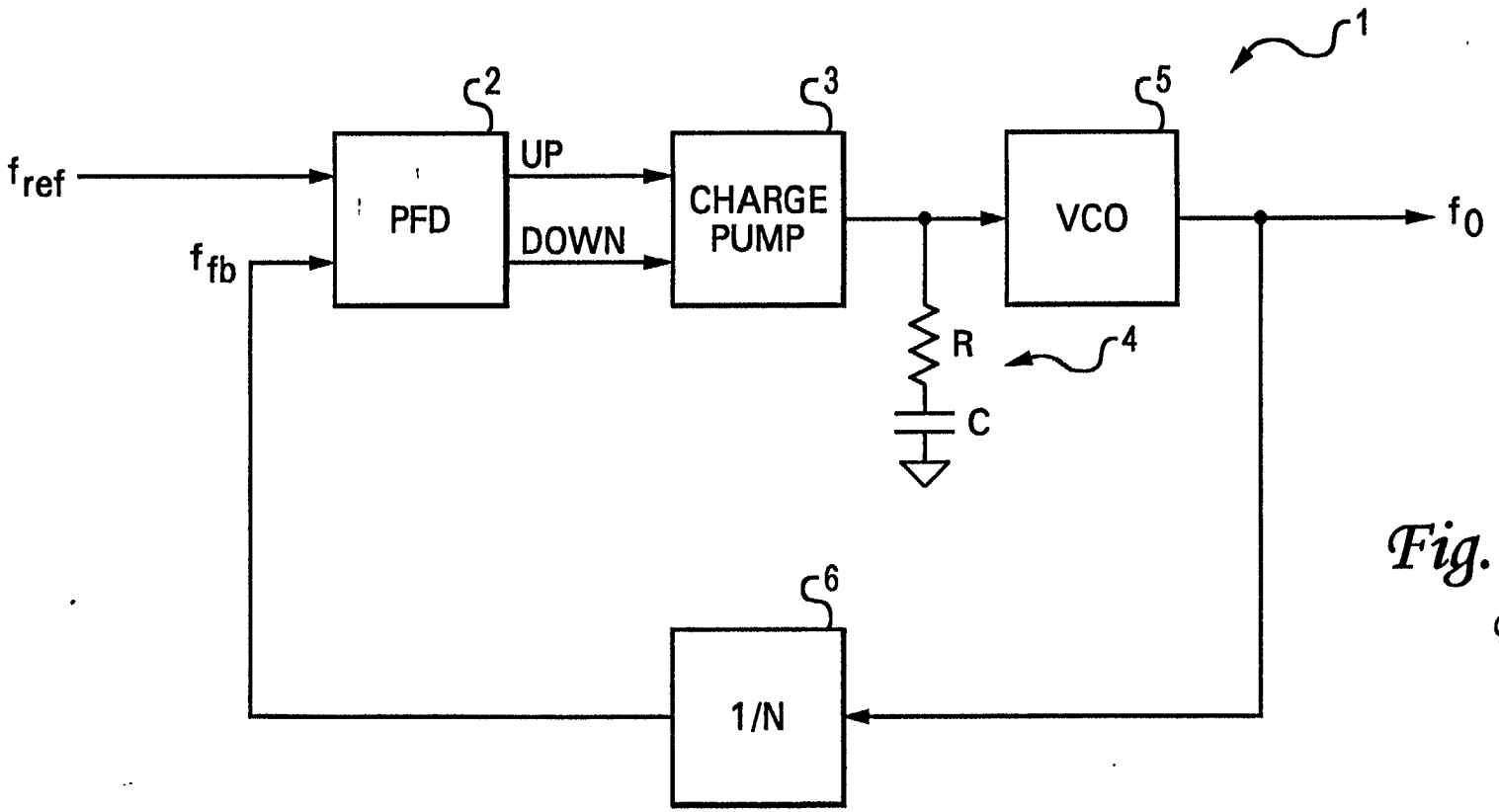
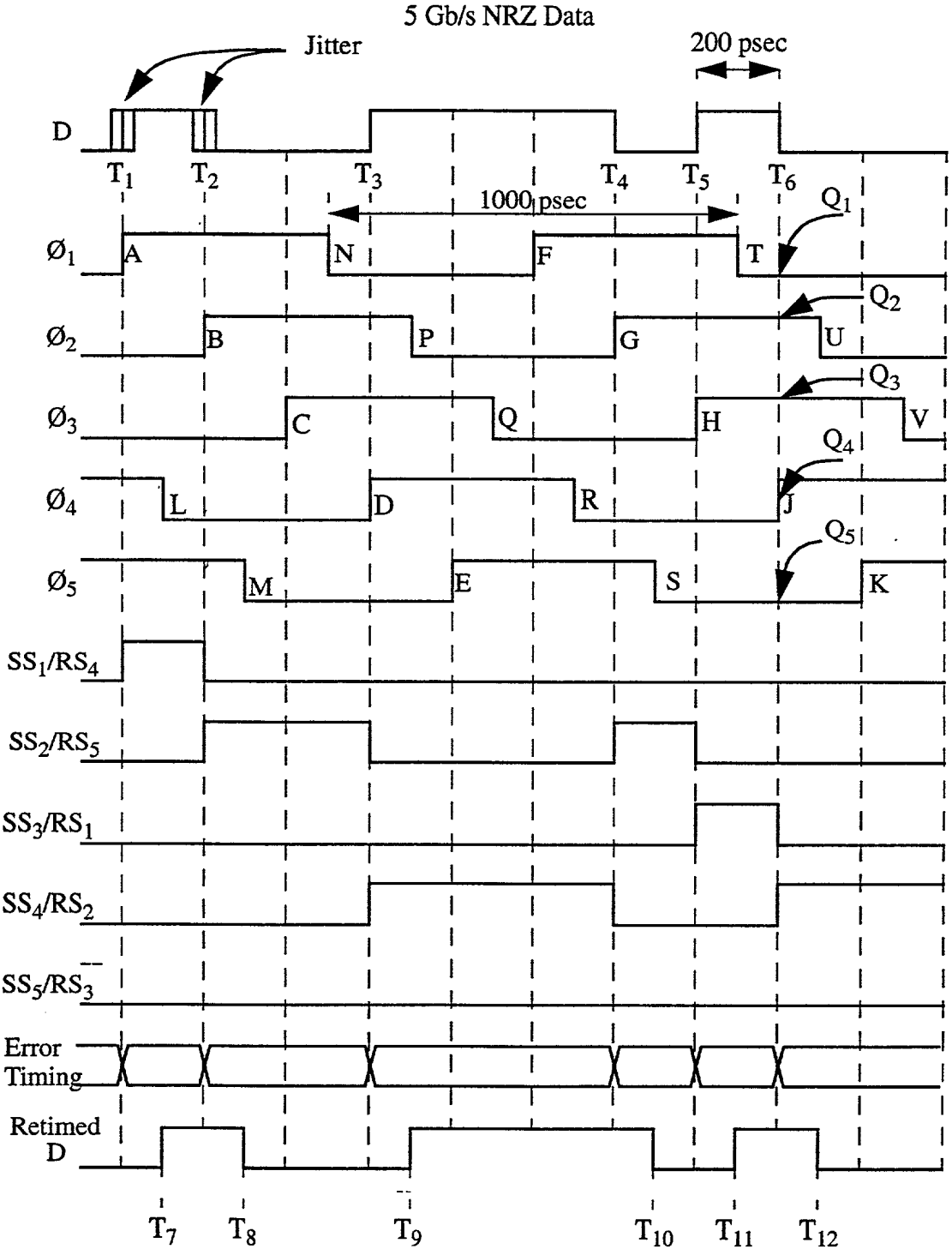


Fig. 1
Prior Art



~~PLL Synchronization and Retiming at 1/5 Data Rate using Multiphase VCO and D-Type PFD~~

Figure ~~#~~ 2

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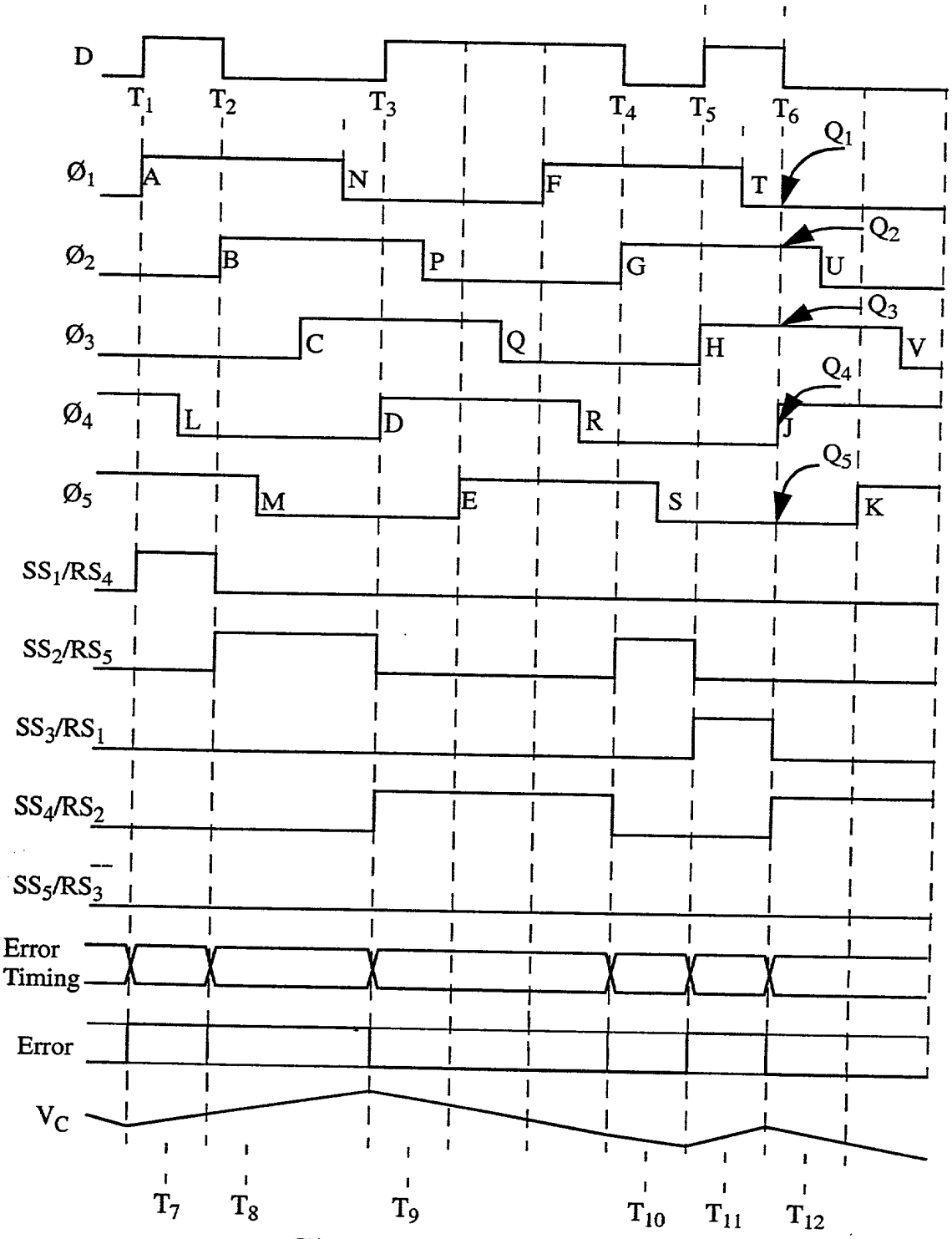
Q_1	Q_2	Q_3	Q_4	Q_5	SynchState	RetimeState
X	0	0	1	1	1	4
1	X	0	0	1	2	5
1	1	X	0	0	3	1
0	1	1	X	0	4	2
0	0	1	1	X	5	3

TABLE 1: Synchronization and Retiming State Identification Fig. 3

SynchState	Q_1	Q_2	Q_3	Q_4	Q_5	Clock Late wrt Data
1	0	0	0	1	1	1
1	1	0	0	1	1	0
2	1	0	0	0	1	1
2	1	1	0	0	1	0
3	1	1	0	0	0	1
3	1	1	1	0	0	0
4	0	1	1	0	0	1
4	0	1	1	1	0	0
5	0	0	1	1	0	1
5	0	0	1	1	1	0

TABLE 2: Determination of Timing Correction Fig. 4



Clock and Data Aligned

Figure 25

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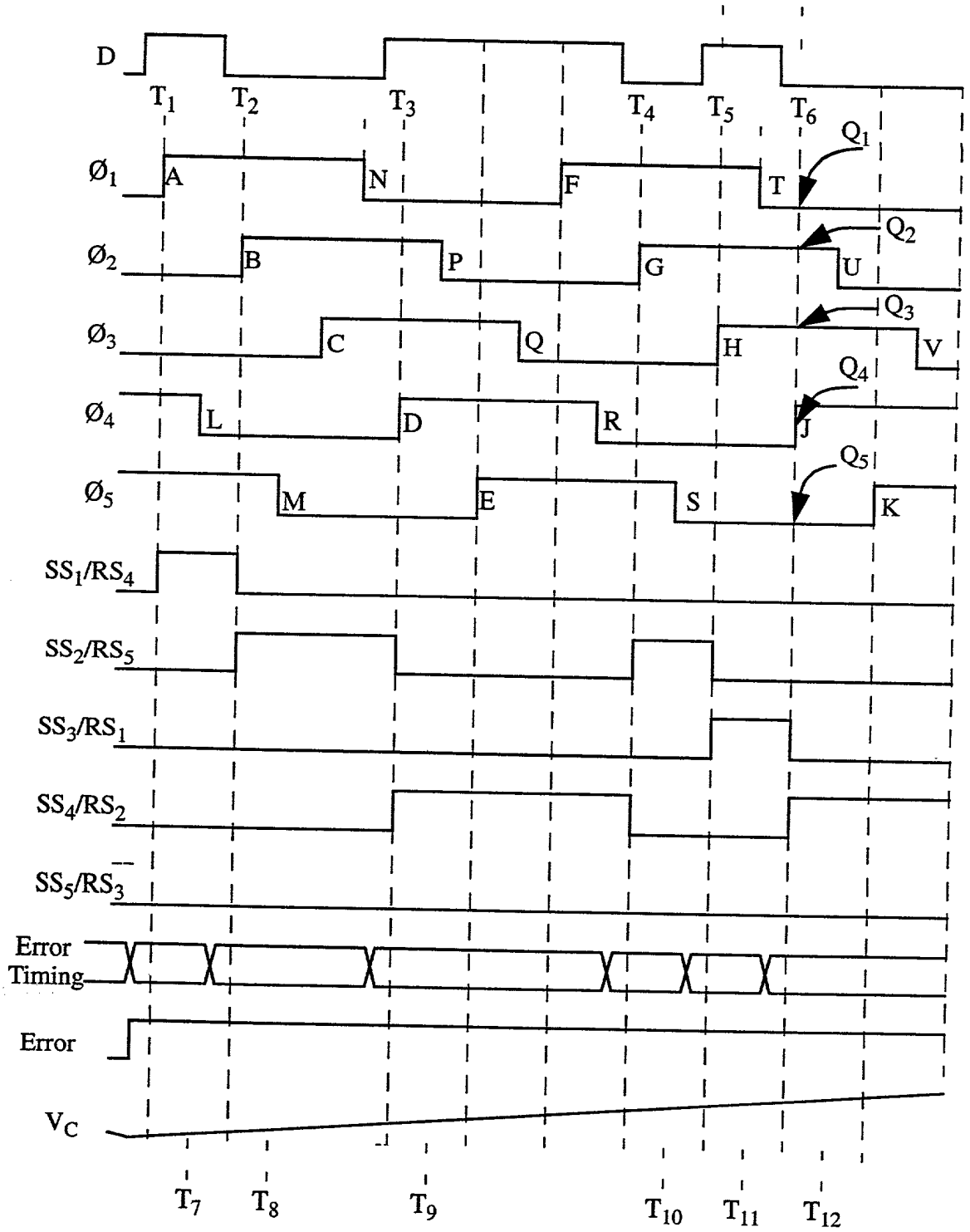

Clock Lags Data

Figure 3 6

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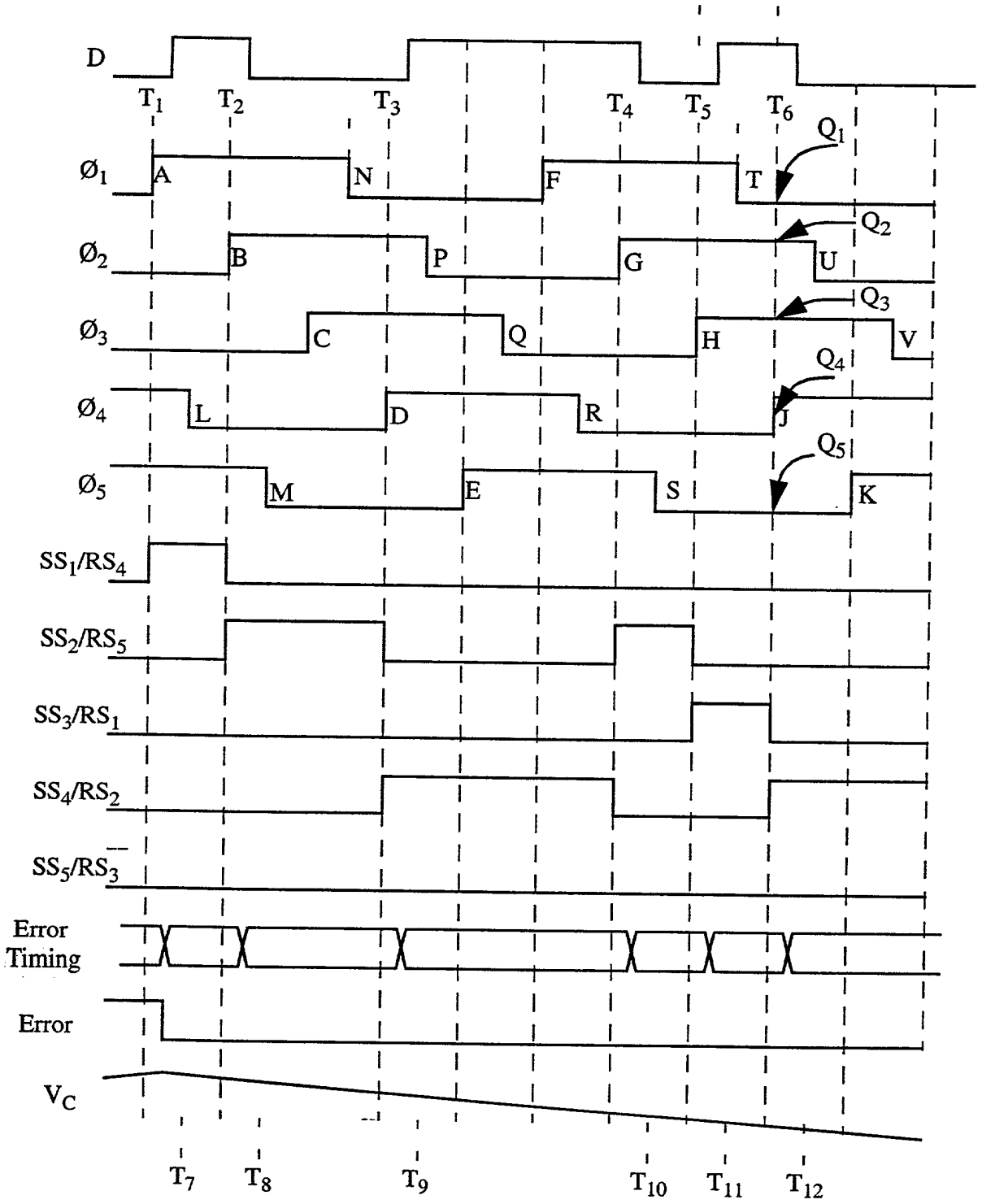

~~Clock Leads Data~~

Figure 4

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~~D Boerstler~~

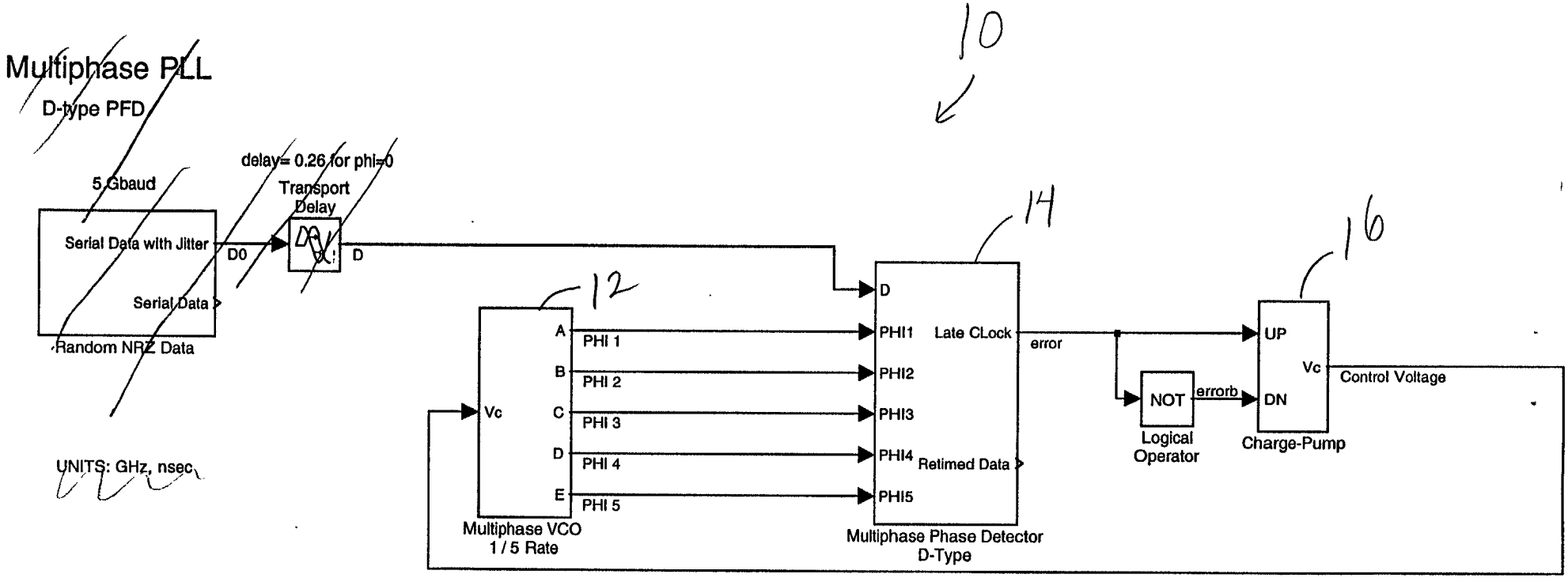


Figure 5: Multiphase PLL using D-type Phase Detector

8

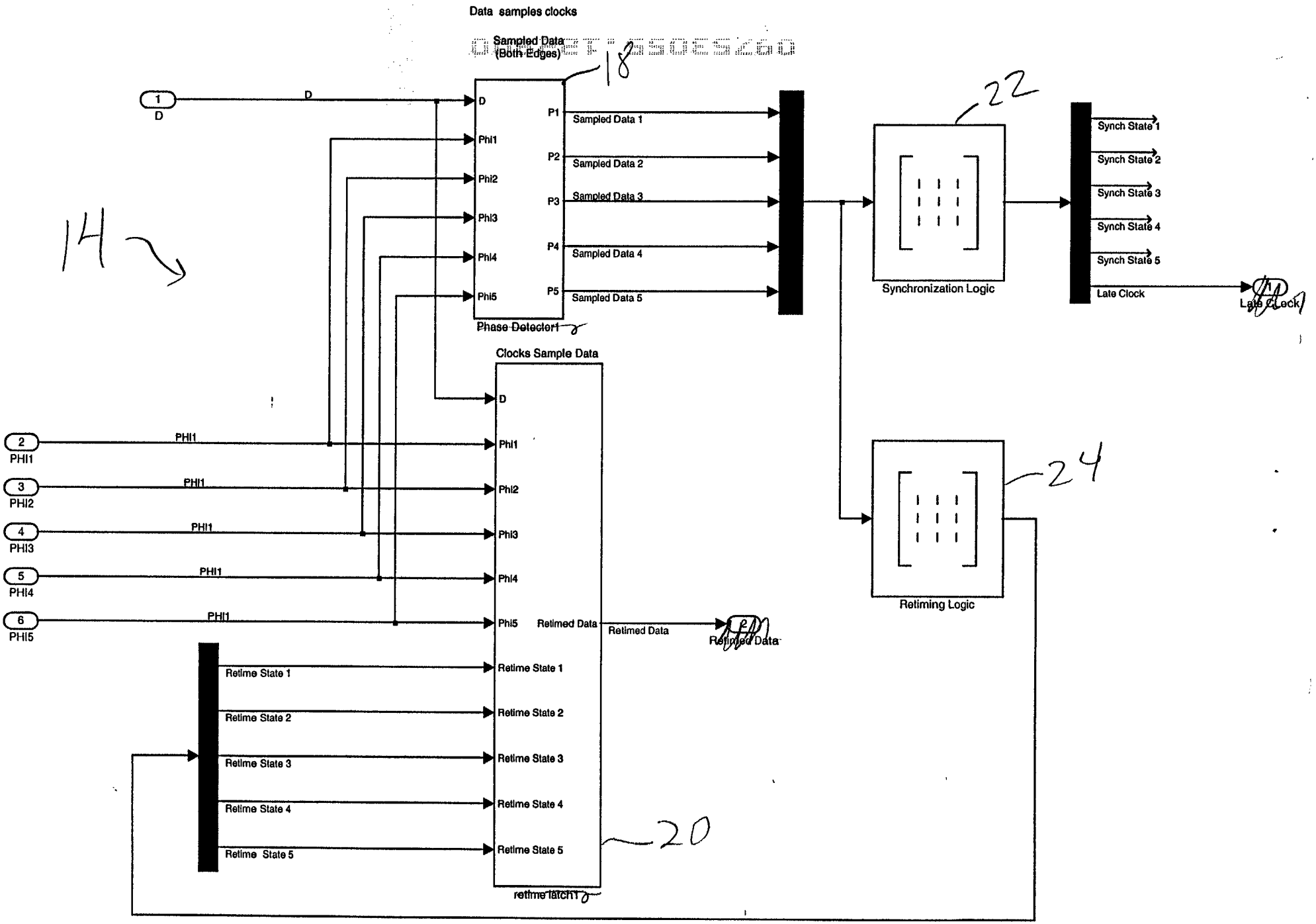


Figure 6; Multiphase Phase Detector D-Type

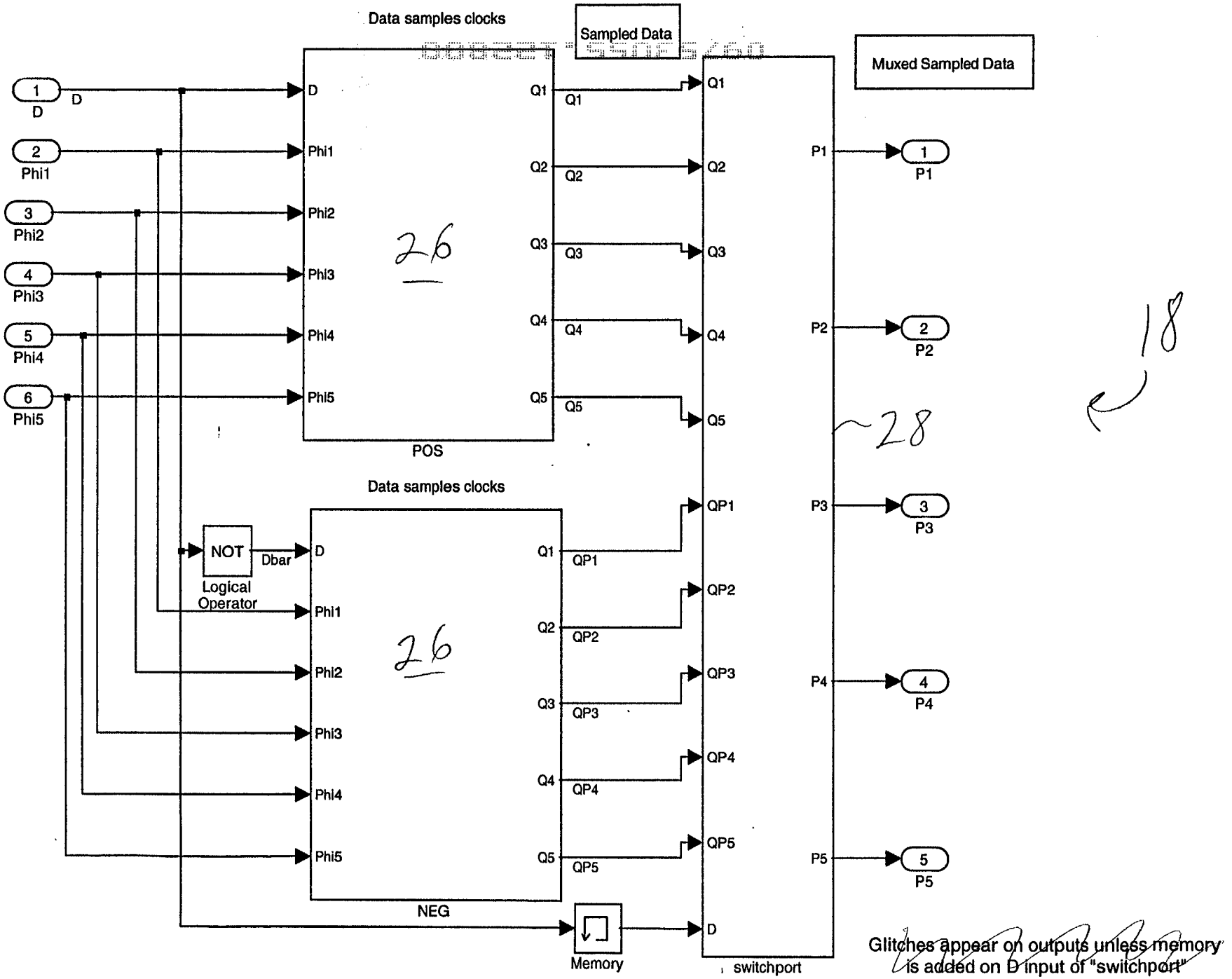


Figure 7: Phase Detector 1

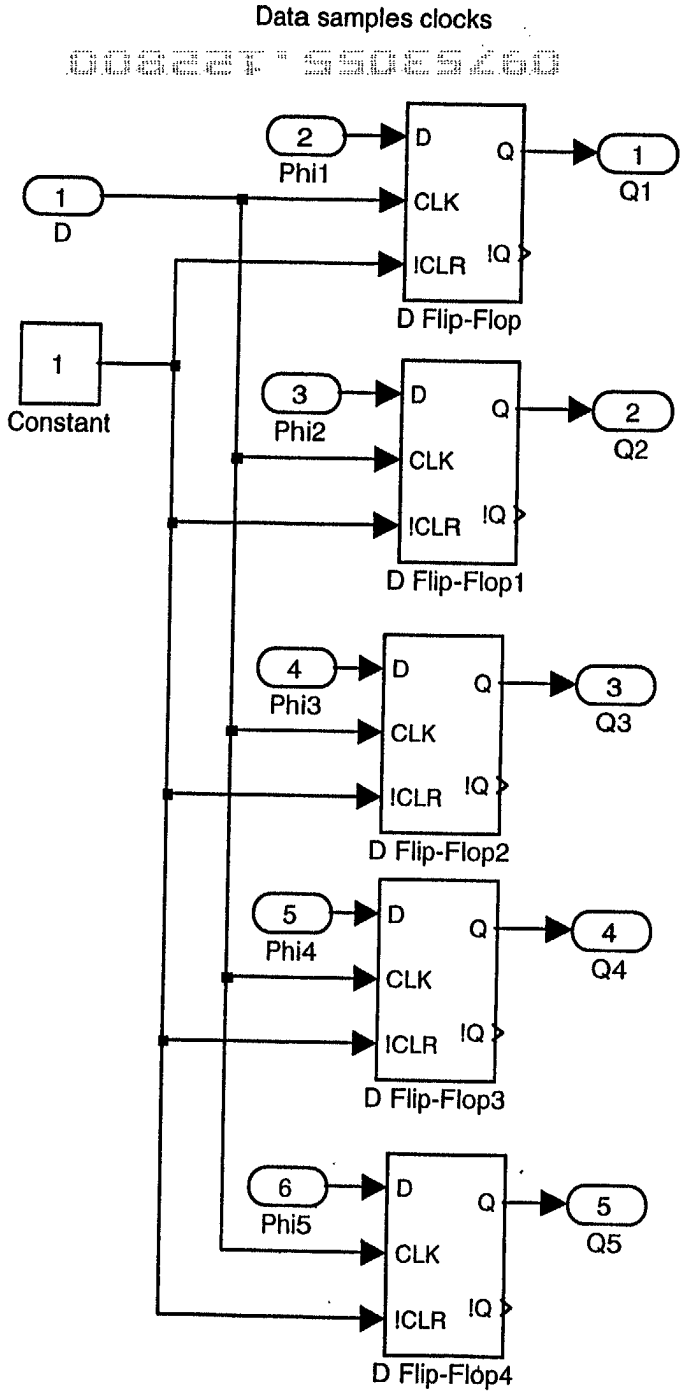
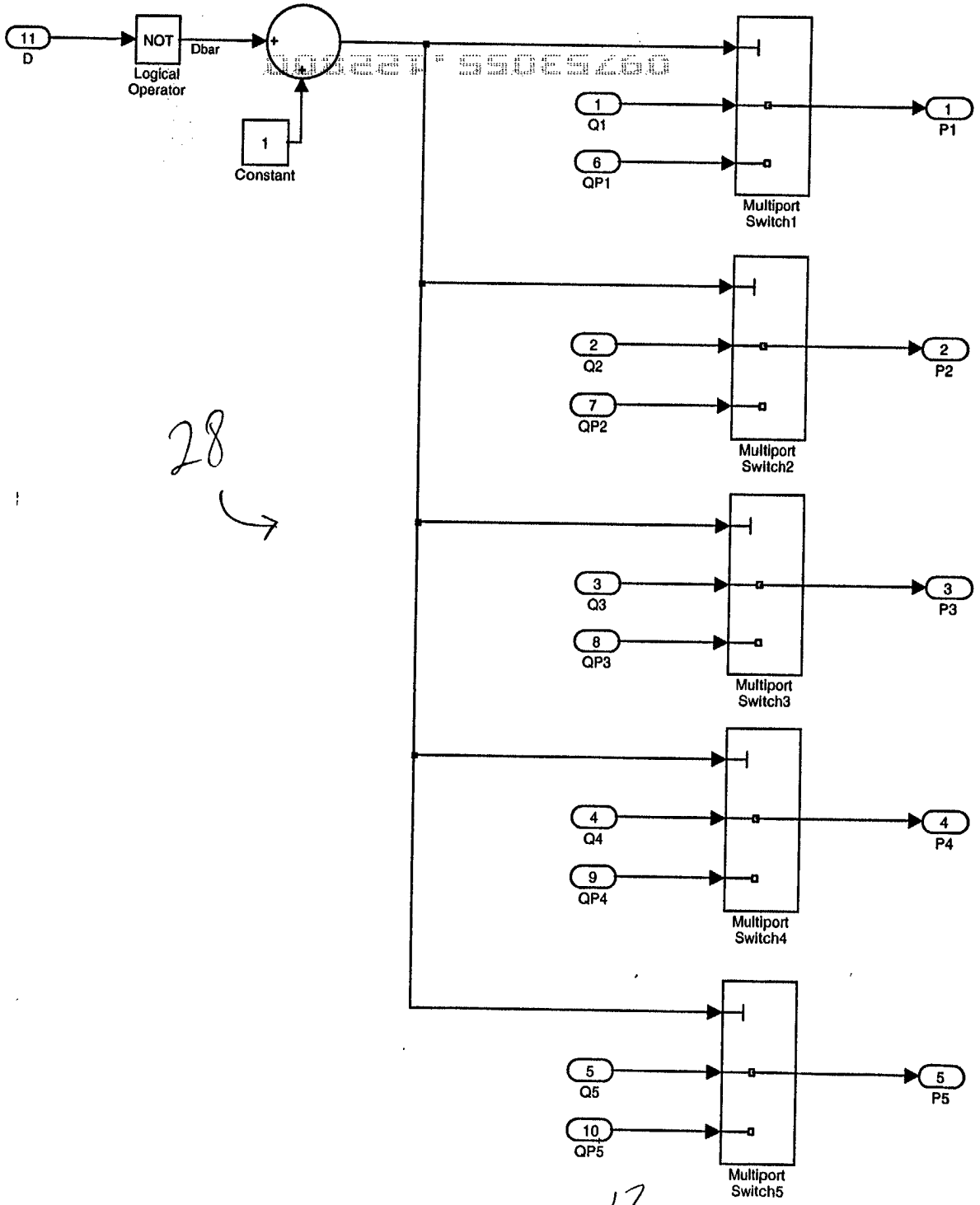


Figure 8. POS & NEG



28

12

Figure 9: Switchport

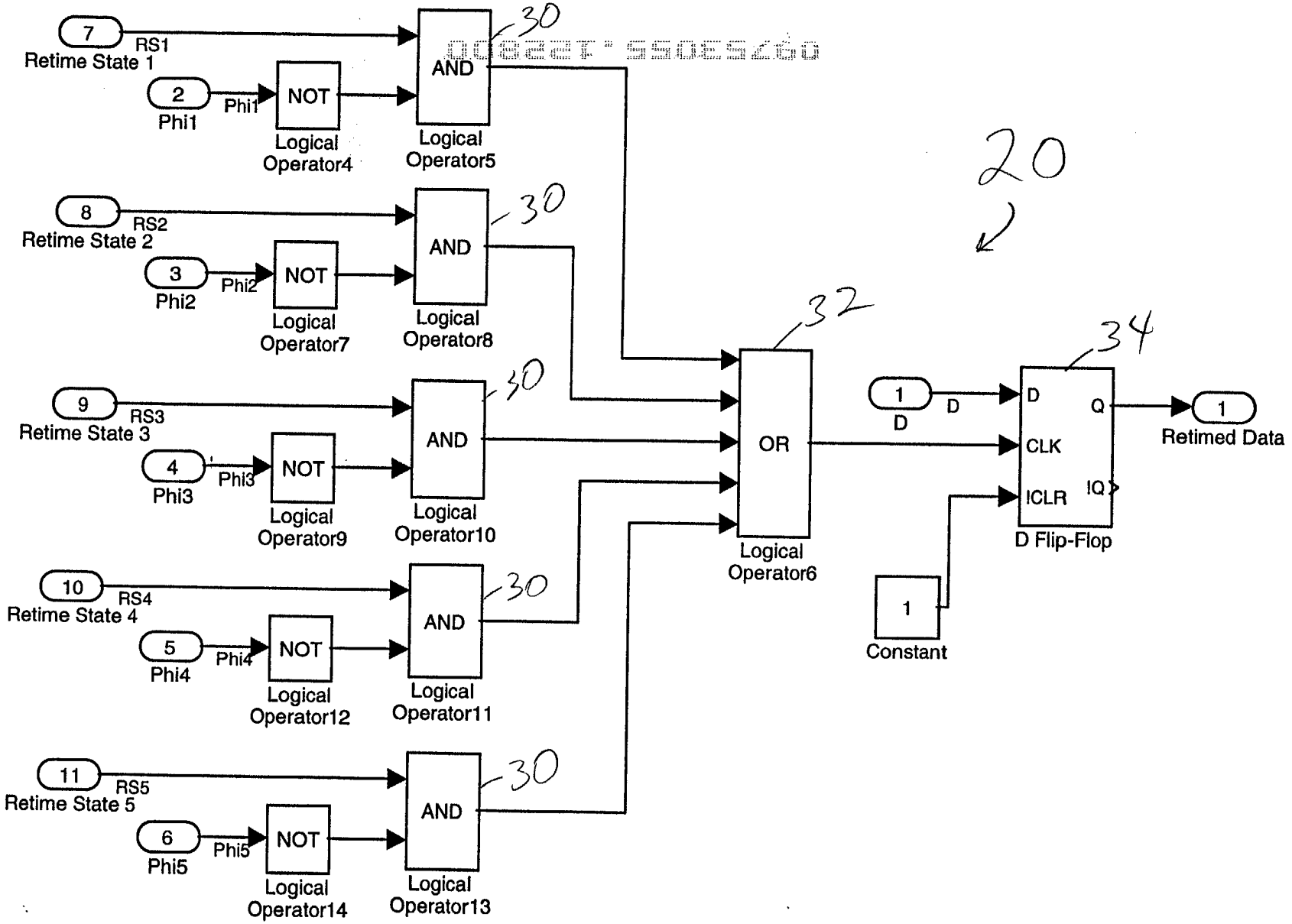


Figure 3: Retime Latch

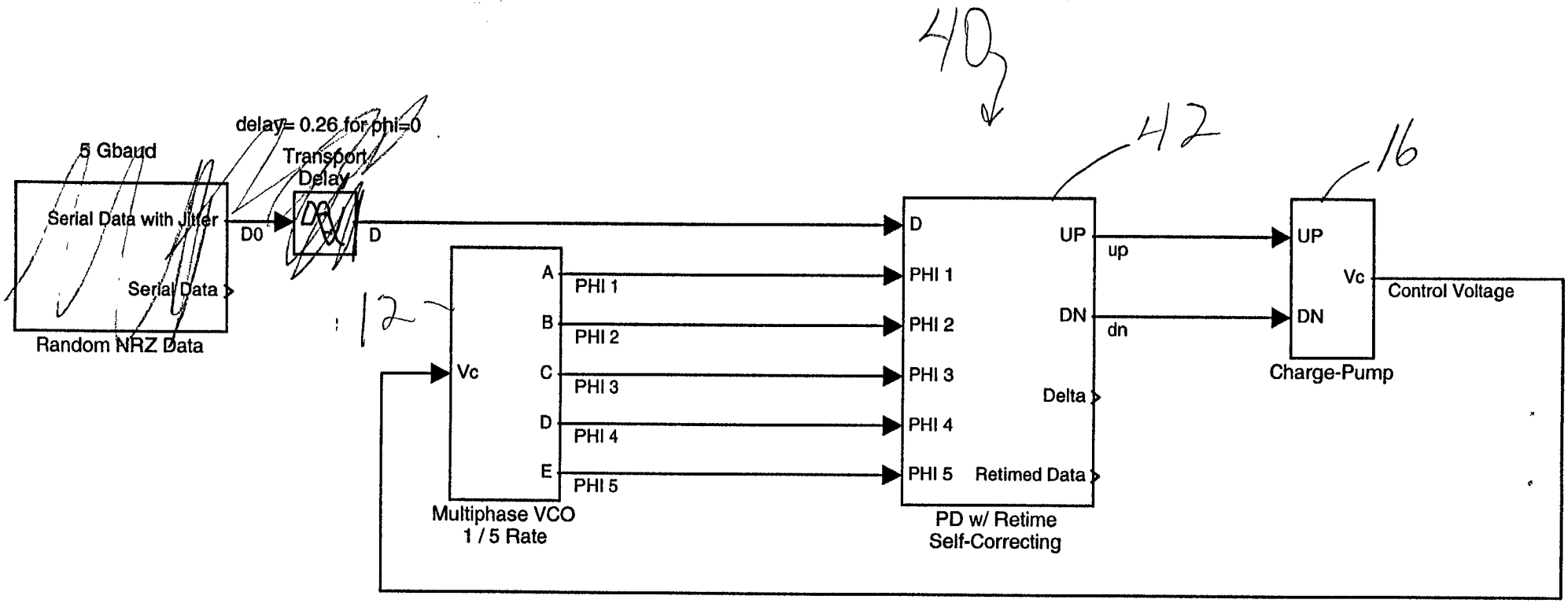


Figure 10: Multiphase PLL using Self-Correcting PD

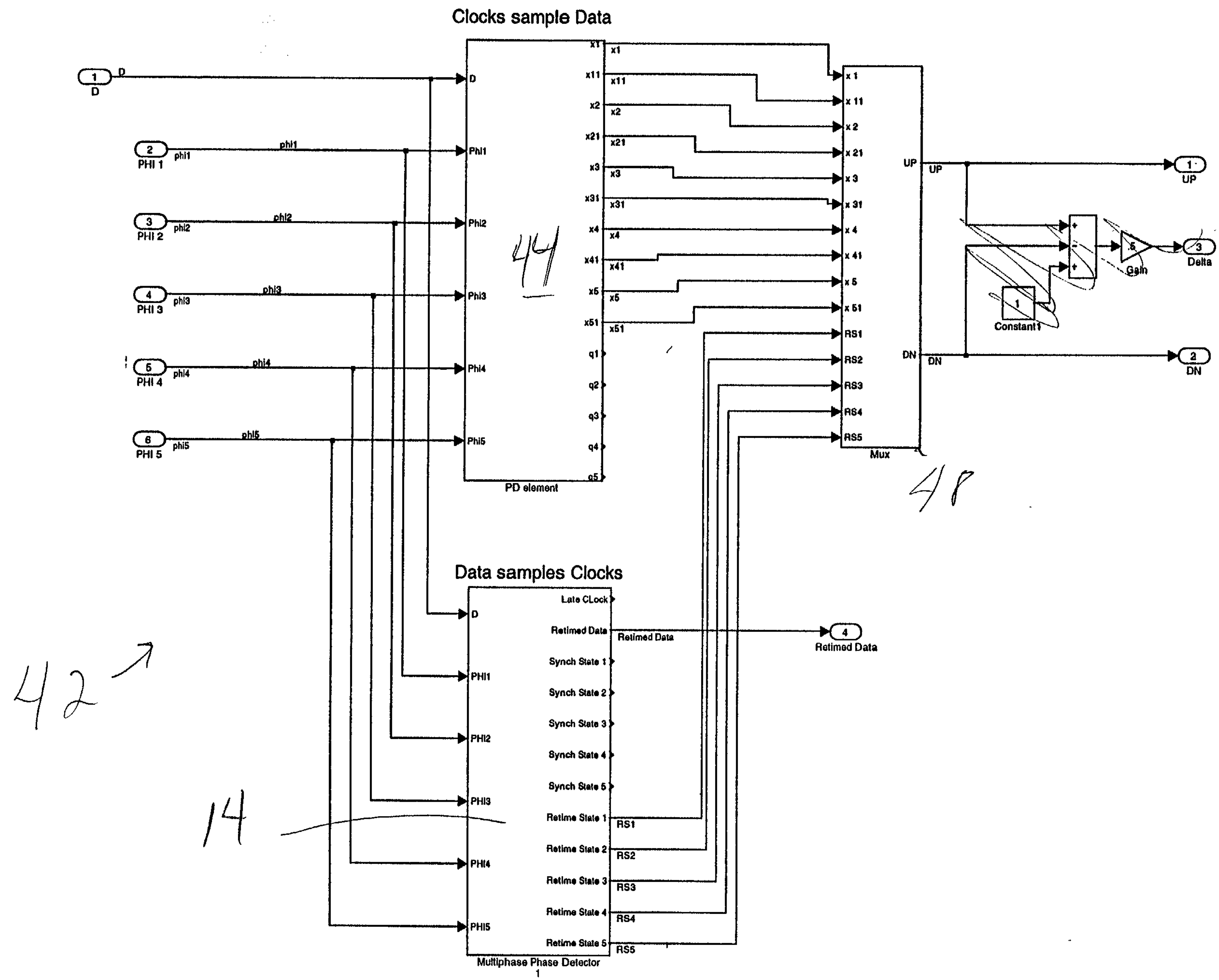
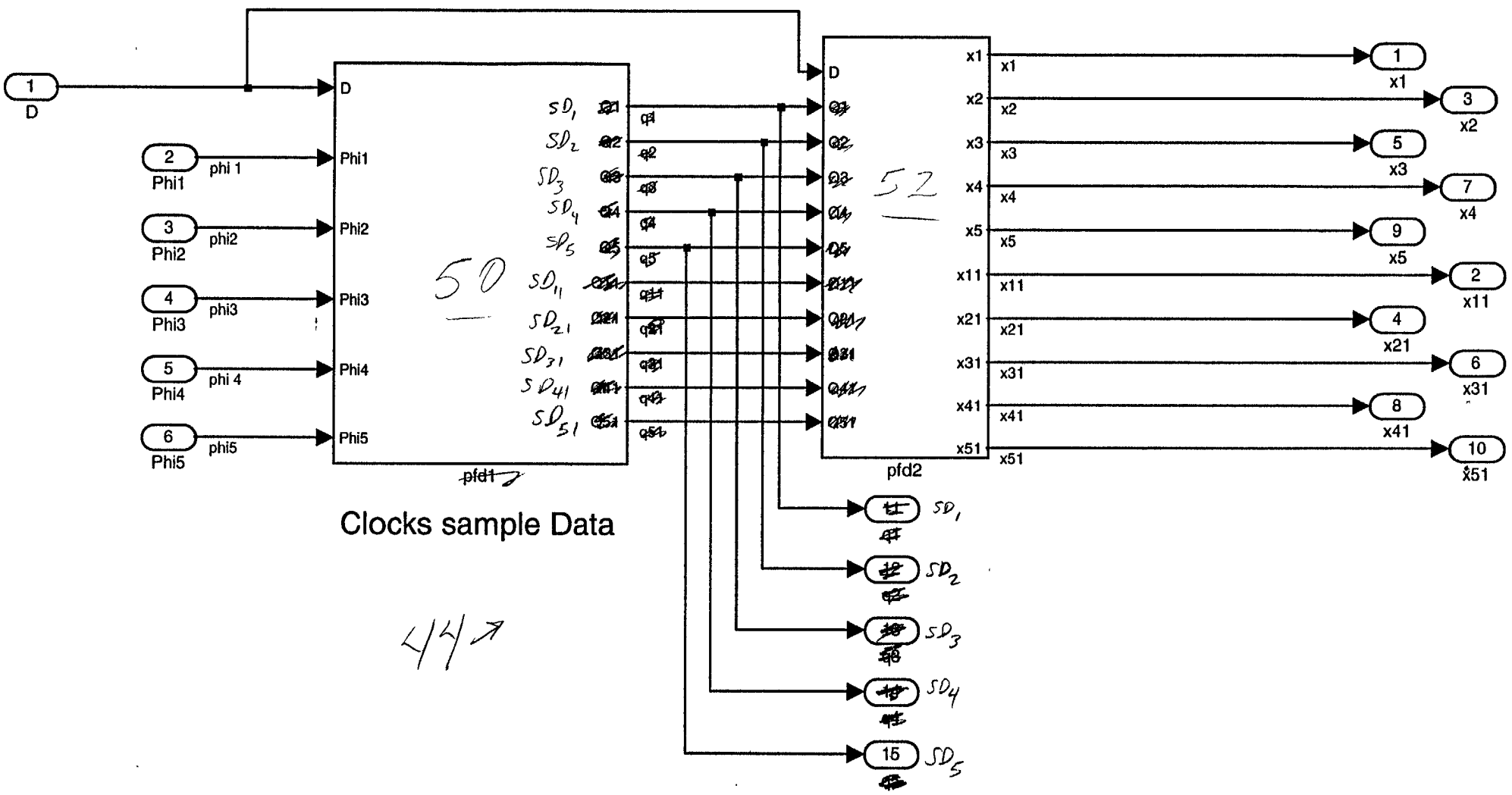


Figure ~~11~~ 5: ~~Multiphase PD with Retime~~



Clocks sample Data

Figure 12: PD Element

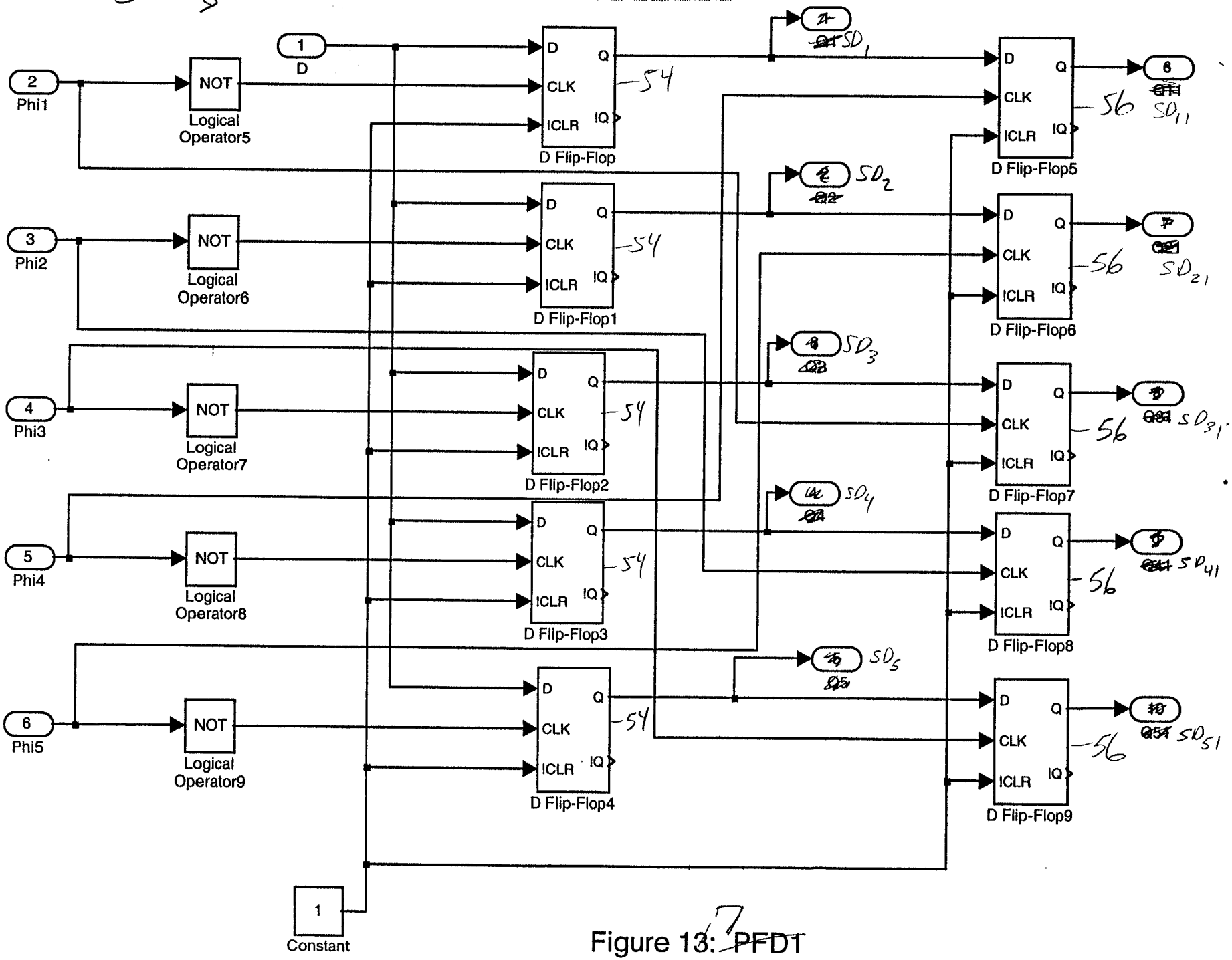


Figure 13: PFD1

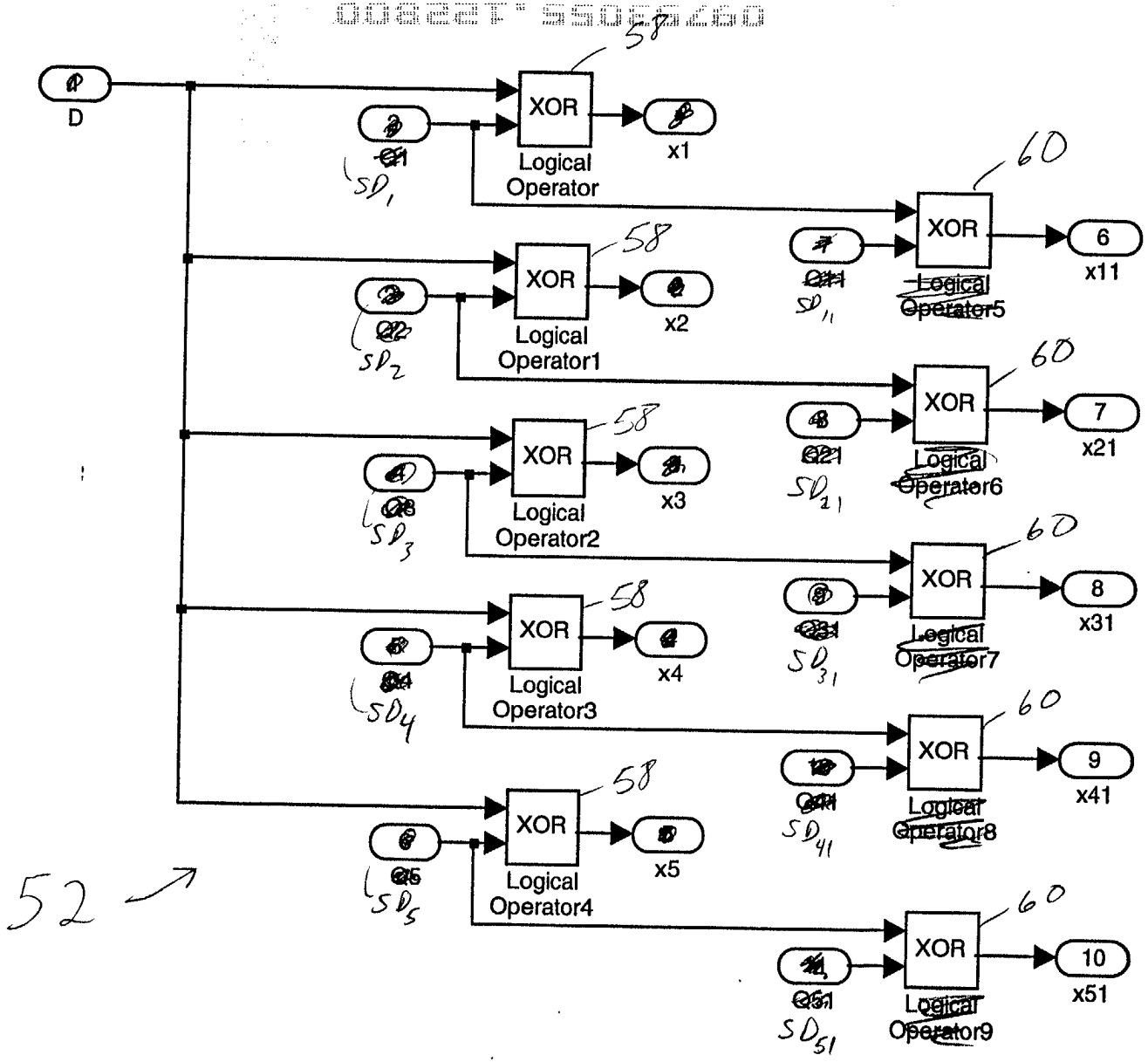


Figure 14: PFD2

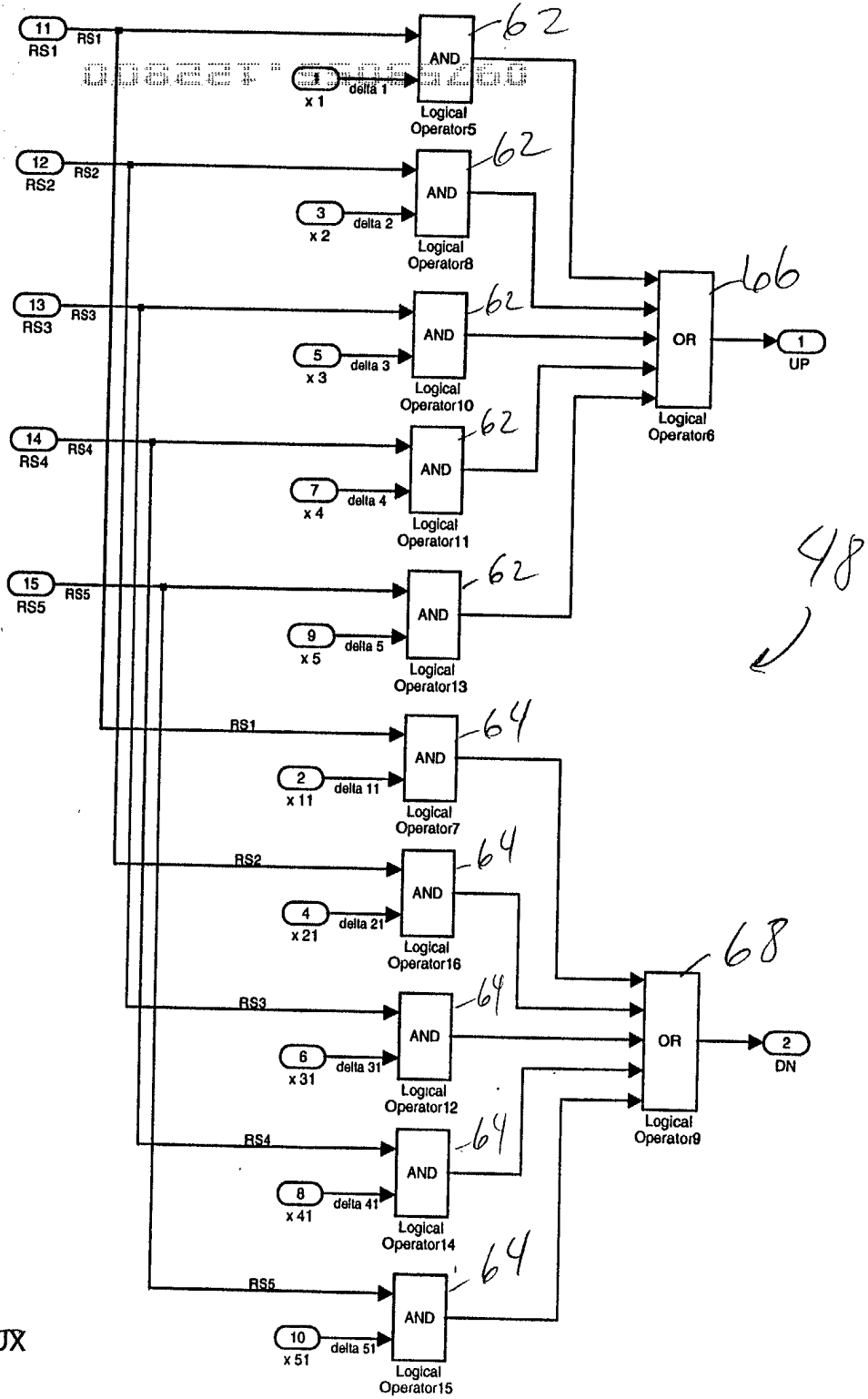
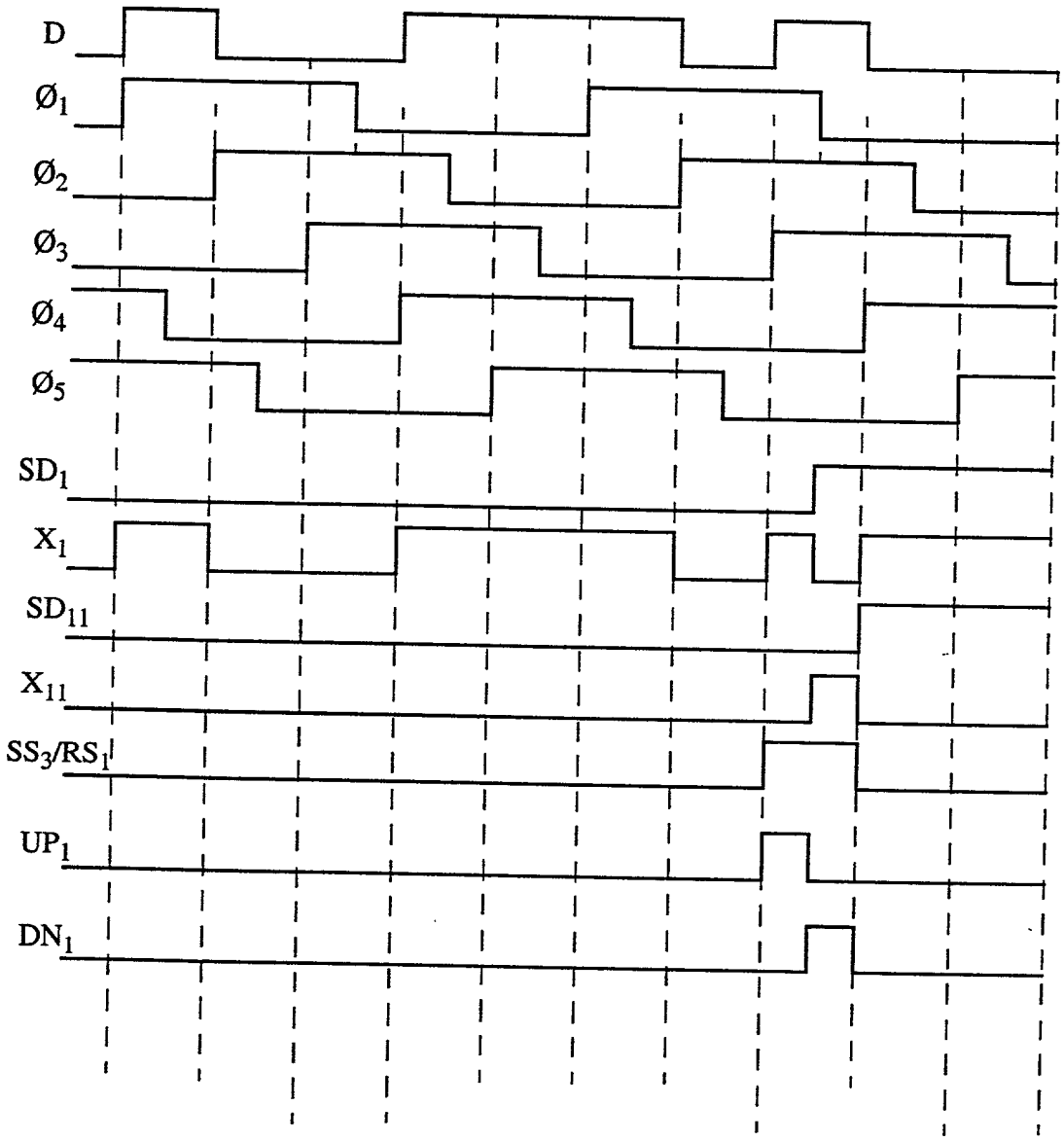


Figure 15: MUX



~~Retime State 1 Timing~~
~~Clock and Data Aligned~~

Figure ~~2~~ 20

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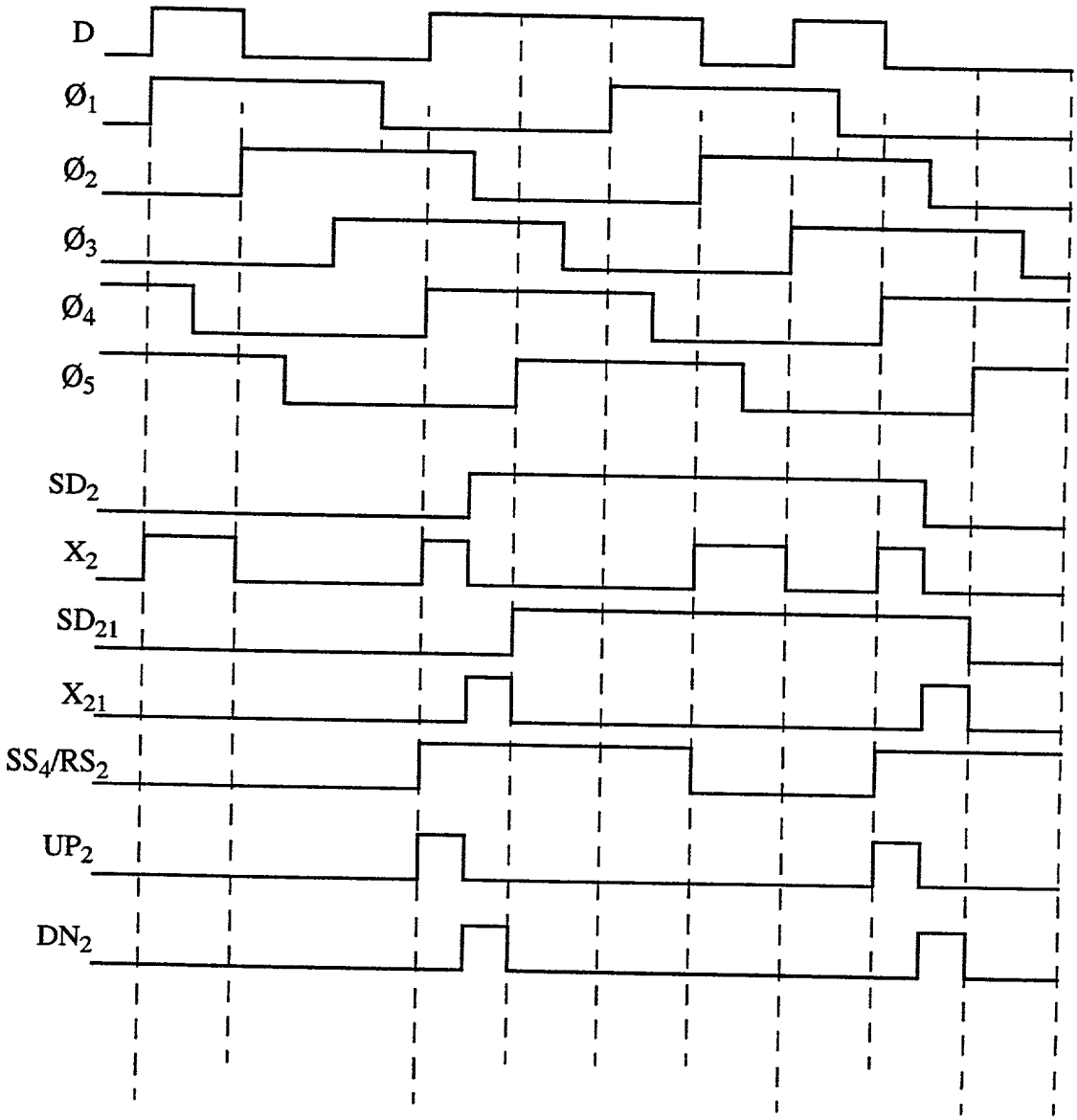

~~Retime State 2 Timing~~
~~Clock and Data Aligned~~

Figure ~~3~~ 21

~~May 2, 2000~~

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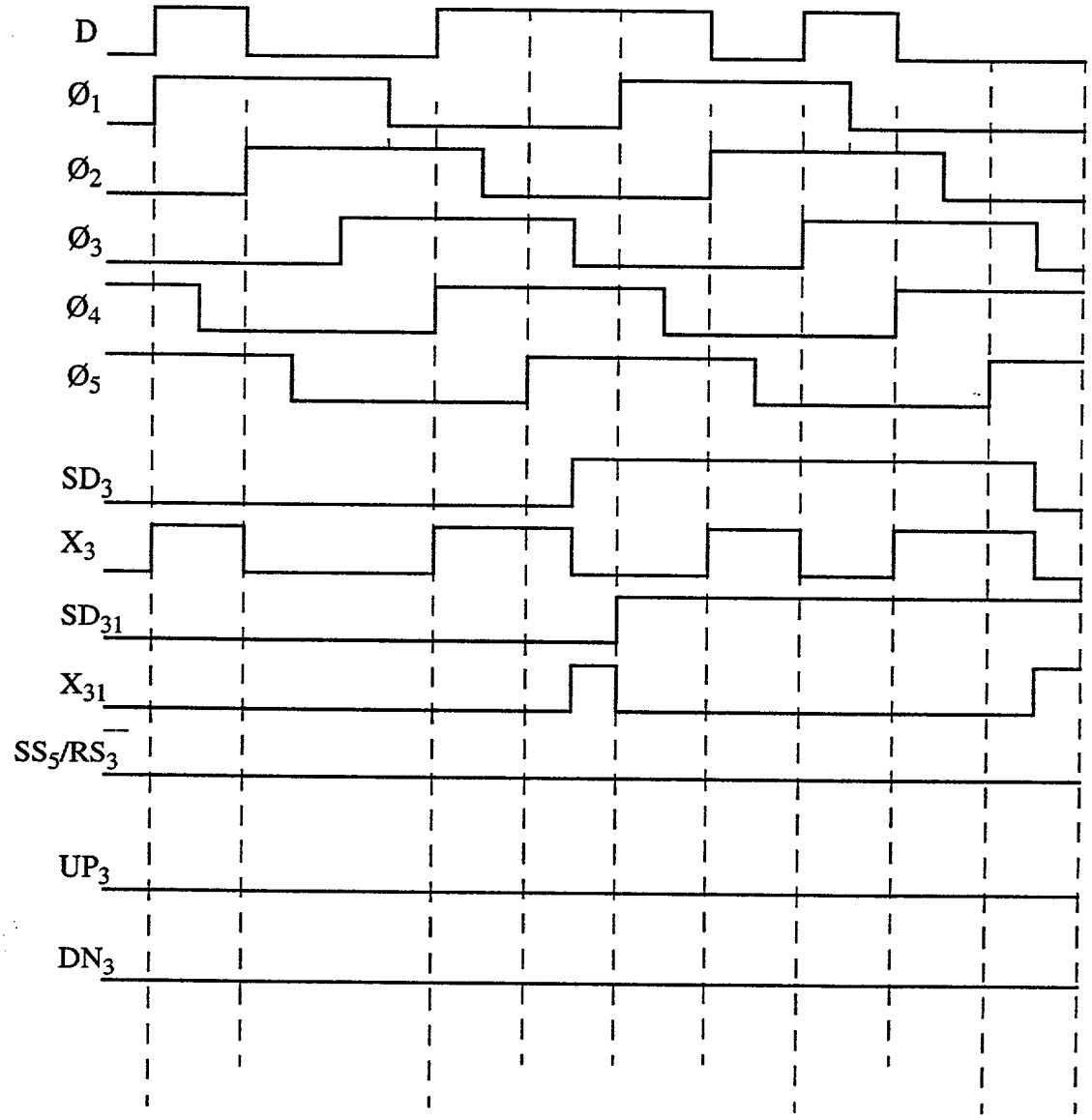
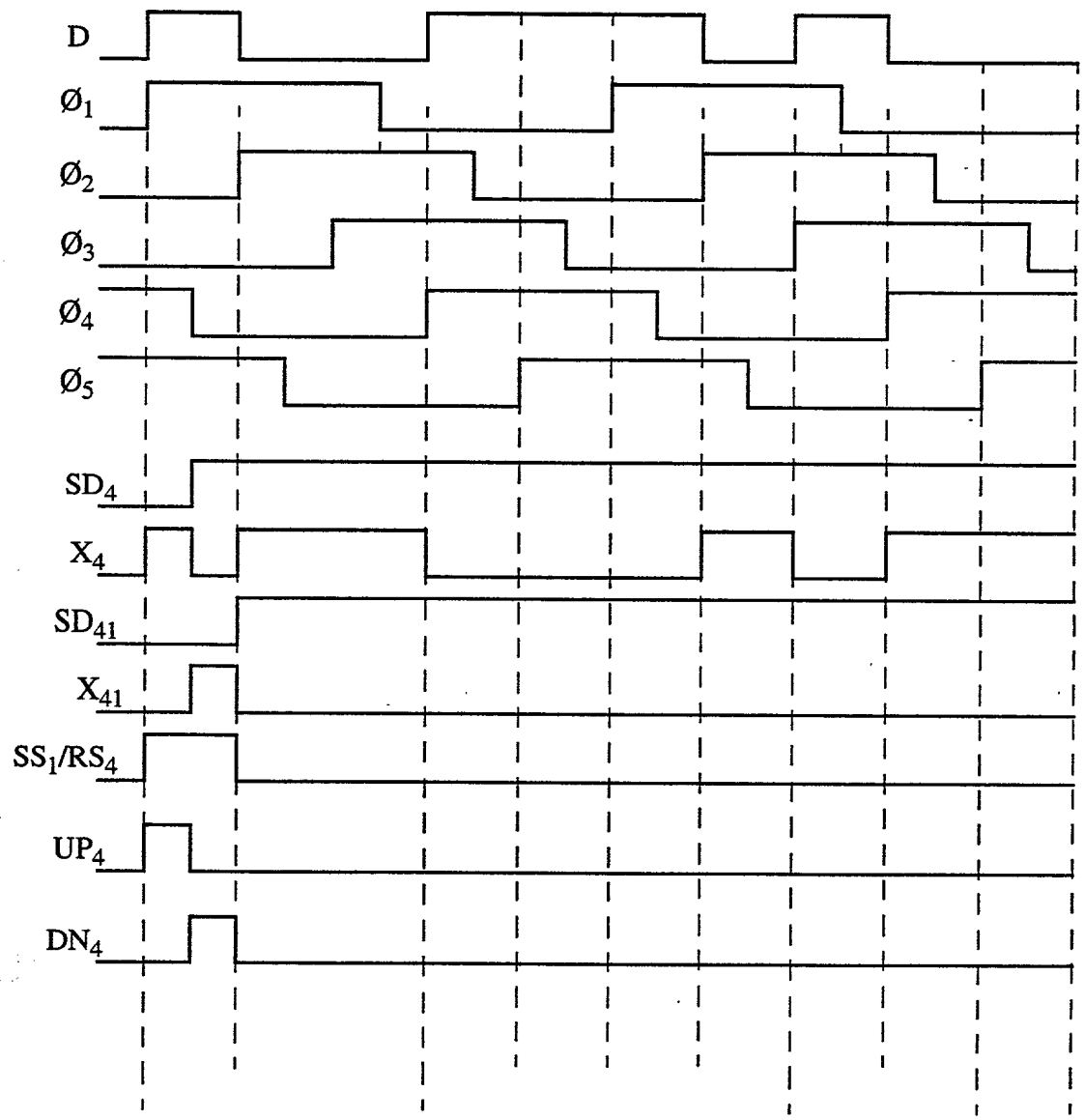


~~Retime State 3 Timing~~
~~Clock and Data Aligned~~

Figure ~~4~~ 22



~~Retime State 4 Timing~~
~~Clock and Data Aligned~~

Figure 5 23

~~May 2, 2000~~

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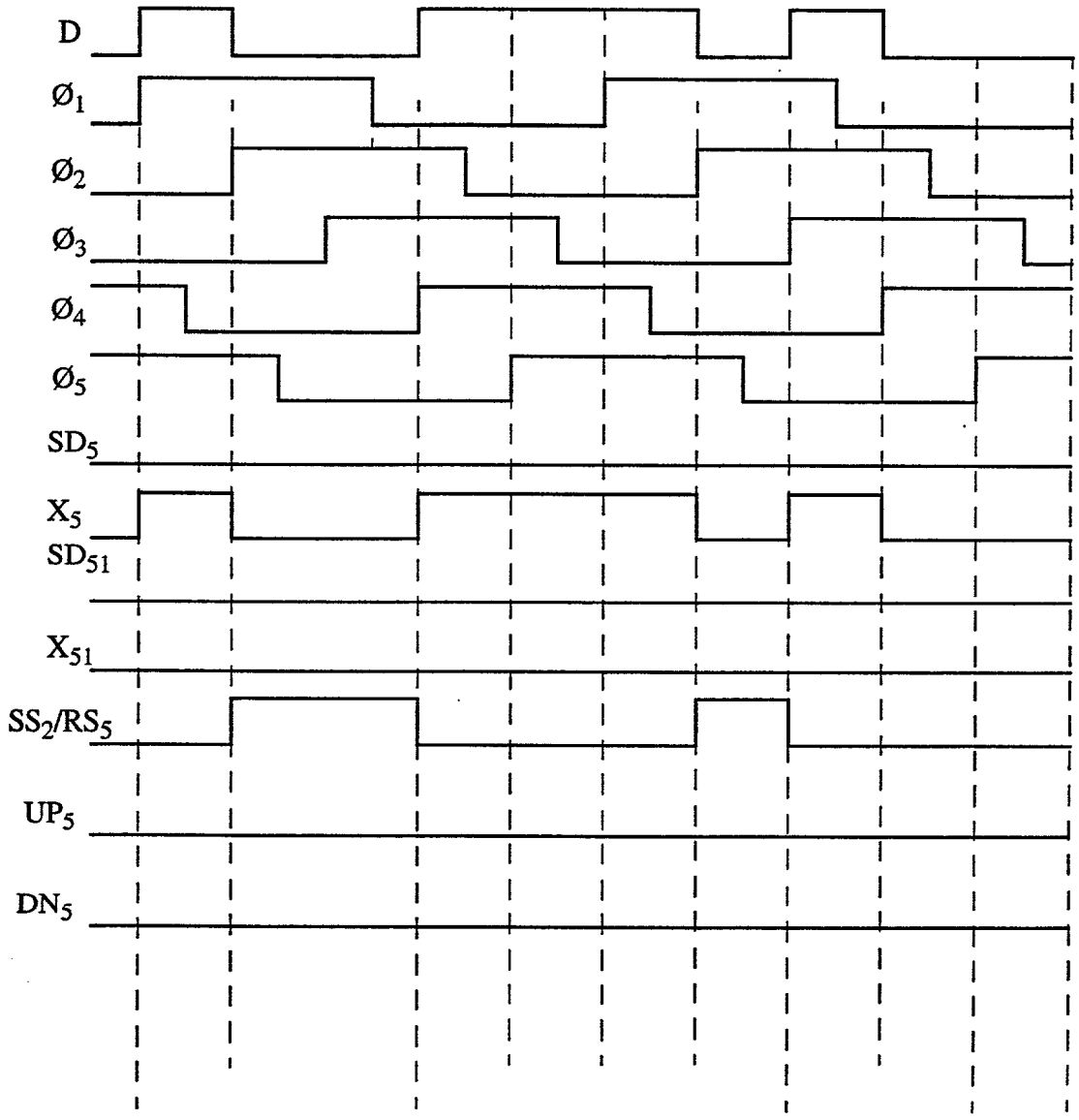
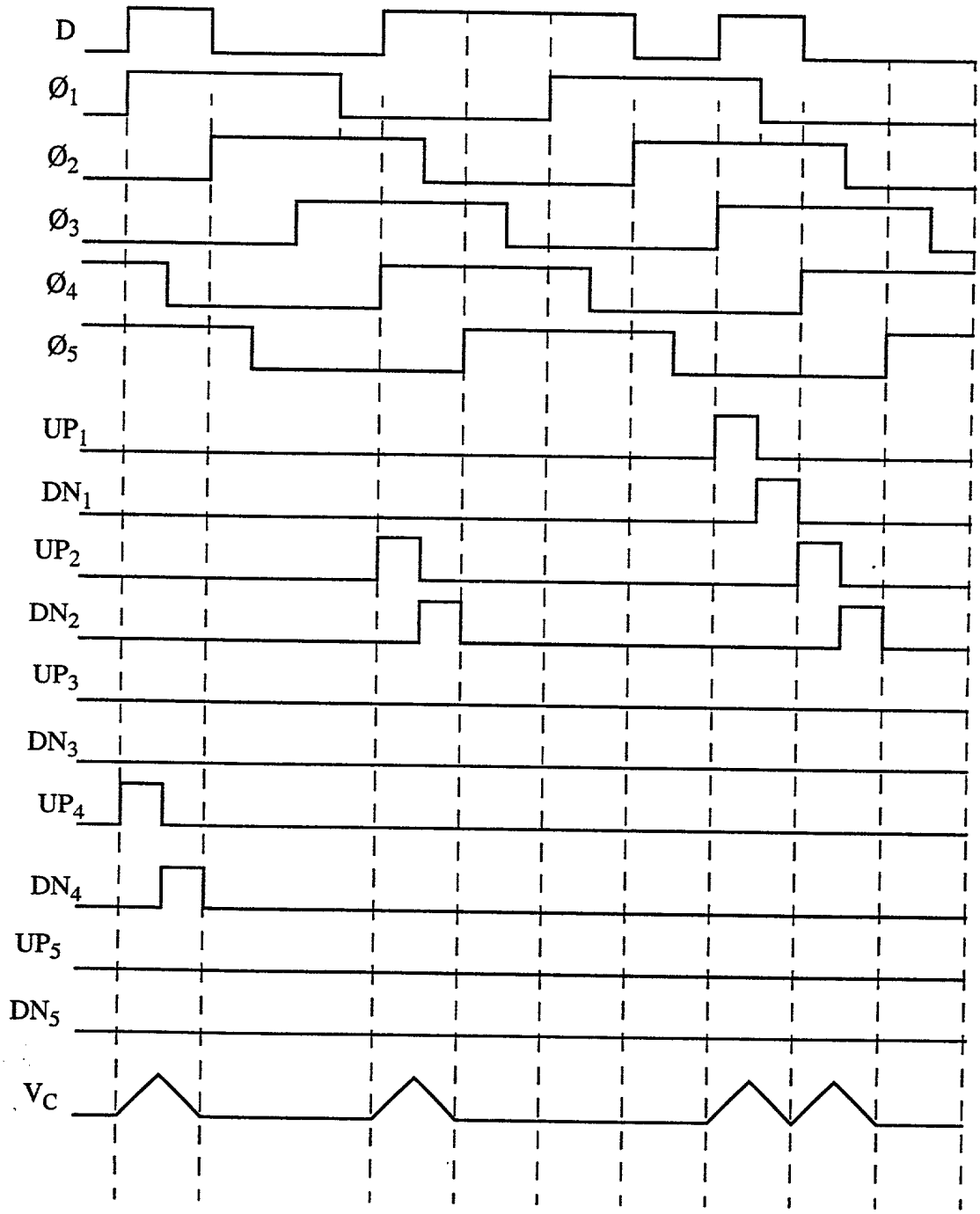


~~Retime State 5 Timing~~
~~Clock and Data Aligned~~

Figure ~~6~~ 24



~~Clock and Data Aligned~~

Figure 25

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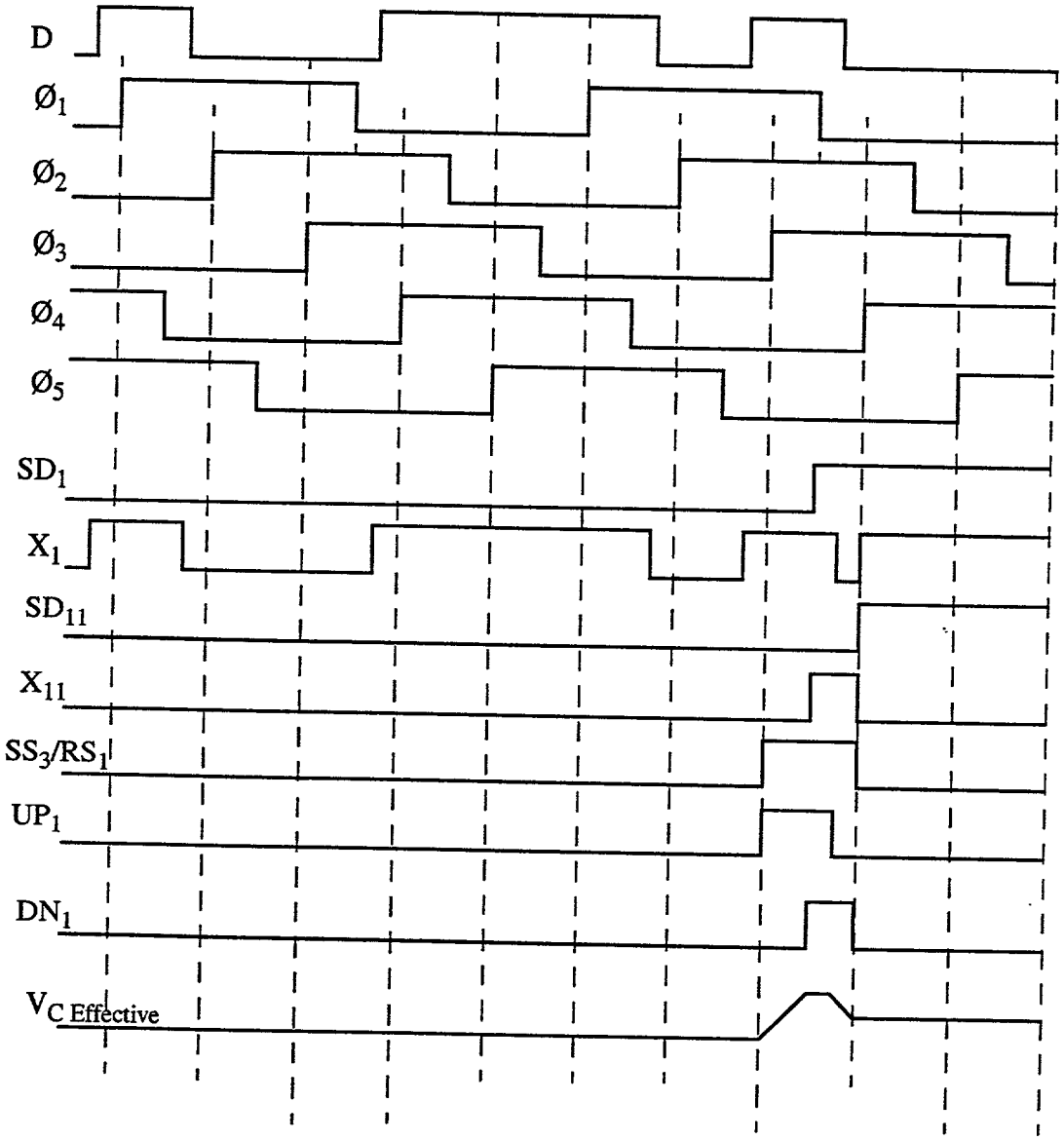
~~D Boerstler~~



Retime State 1 Timing

Clock Lags Data

Figure 8 26

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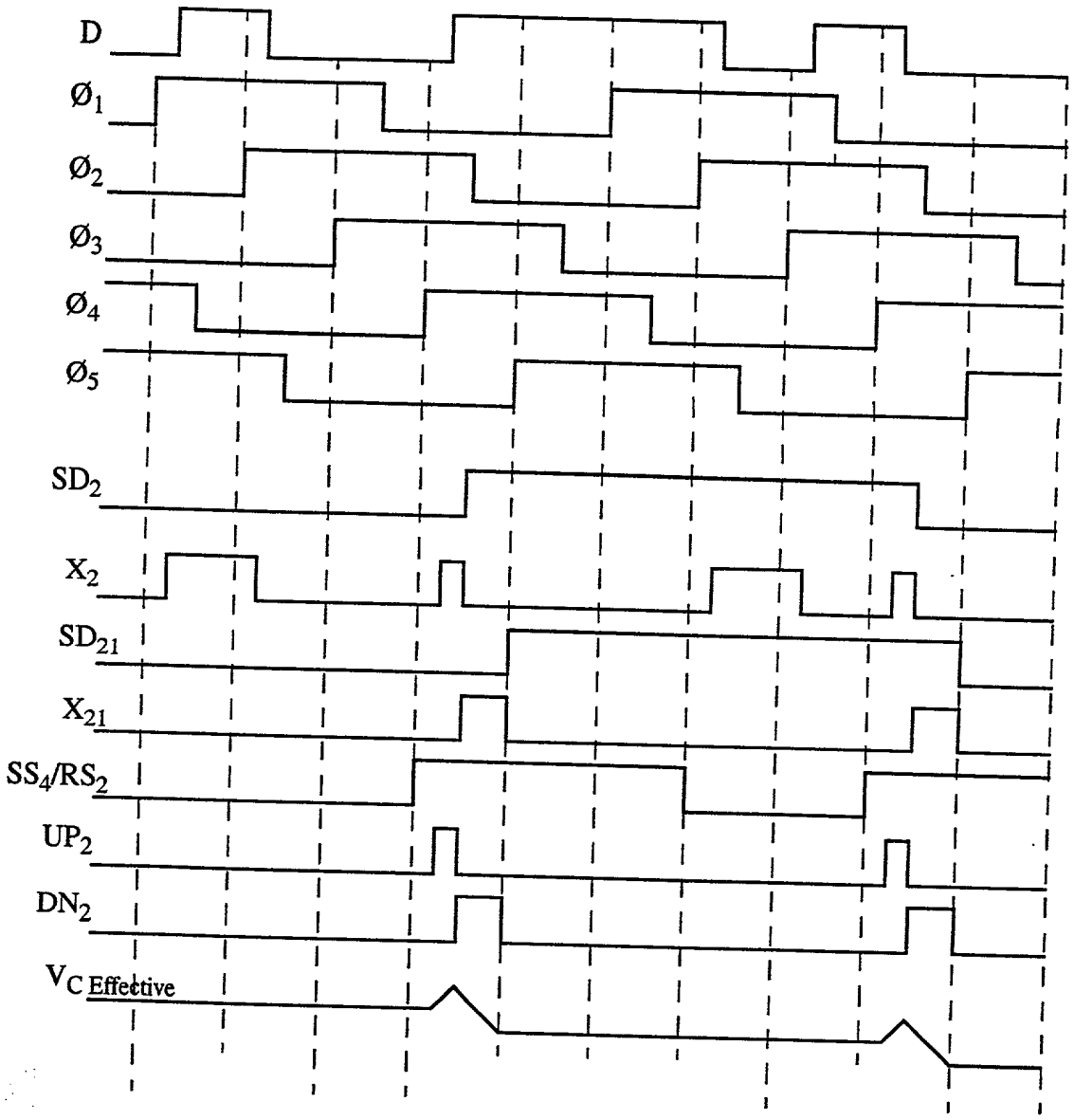

~~Retime State 2 Timing~~
~~Clock Leads Data~~

Figure 9 27

~~May 2, 2000~~

~~D Boerstler~~